



# 1.8V PHASE LOCKED LOOP DIFFERENTIAL 1:10 SDRAM CLOCK DRIVER

IDTCSPUA877A

## FEATURES:

- 1 to 10 differential clock distribution
- Optimized for clock distribution in DDR2 (Double Data Rate) SDRAM applications
- Operating frequency: 125MHz to 410MHz
- Stabilization time: <math><6\mu\text{s}</math>
- Very low skew: <math>\leq 40\text{ps}</math>
- Very low jitter: <math>\leq 40\text{ps}</math>
- 1.8V AVDD and 1.8V VDDO
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Available in 52-Ball VFBGA and 40-pin VFQFPN packages

## APPLICATIONS:

- Meets or exceeds JEDEC standard CUA877 for registered DDR2 clock driver
- Along with SSTUA32864/66, DDR2 register, provides complete solution for DDR2 DIMMs

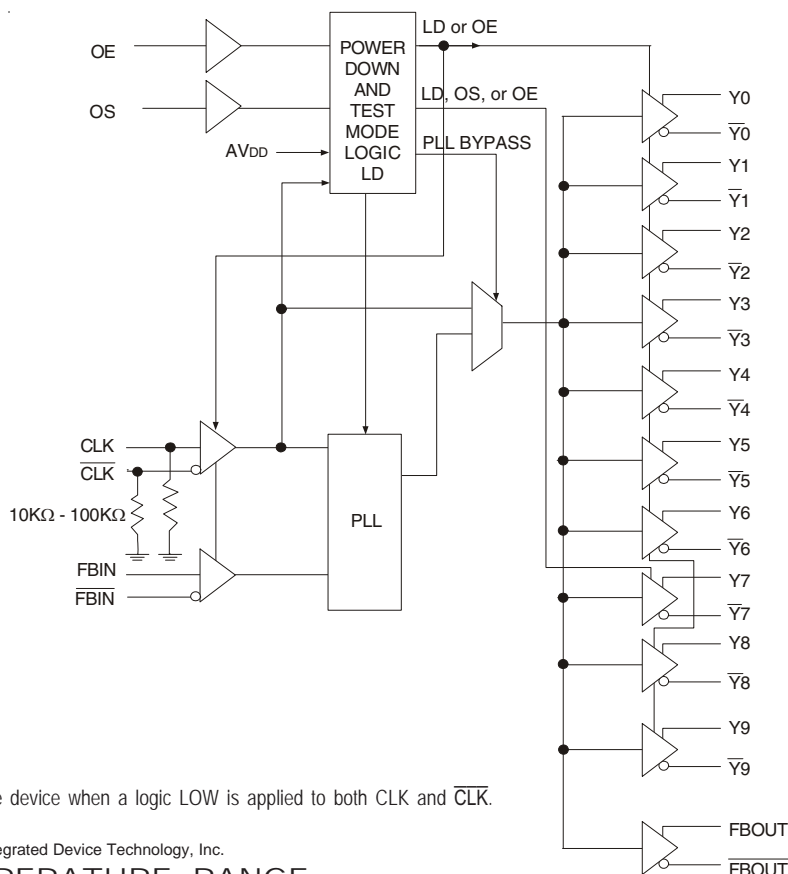
## DESCRIPTION:

The CSPUA877A is a PLL based clock driver that acts as a zero delay buffer to distribute one differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to 10 differential output pairs ( $\overline{\text{Y}}[0:9]$ , Y [0:9]) and one differential pair of feedback clock output (FBOUT,  $\overline{\text{FBOUT}}$ ). External feedback pins (FBIN,  $\overline{\text{FBIN}}$ ) for synchronization of the outputs to the input reference is provided. OE, OS, and AVDD control the power-down and test mode logic. When AVDD is grounded, the PLL is turned off and bypassed for test mode purposes. When the differential clock inputs (CLK,  $\overline{\text{CLK}}$ ) are both at logic low, this device will enter a low power-down mode. In this mode, the receivers are disabled, the PLL is turned off, and the output clock drivers are disabled, resulting in a clock driver current consumption of less than 500 $\mu\text{A}$ .

The CSPUA877A requires no external components and has been optimized for very low phase error, skew, and jitter, while maintaining frequency and duty cycle over the operating voltage and temperature range. The CSPUA877, designed for use in both module assemblies and system motherboard based solutions, provides an optimum high-performance clock source.

The CSPUA877A is available in Commercial Temperature Range (0°C to +70°C). See Ordering Information for details.

## FUNCTIONAL BLOCK DIAGRAM



### NOTE:

The Logic Detect (LD) powers down the device when a logic LOW is applied to both CLK and  $\overline{\text{CLK}}$ .

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COMMERCIAL TEMPERATURE RANGE

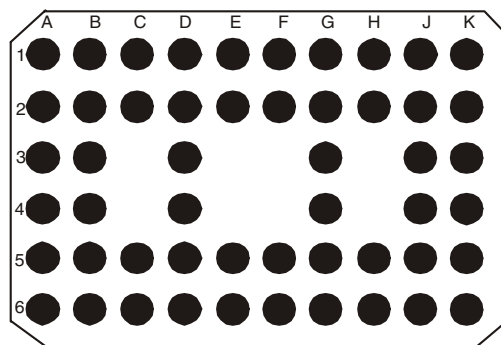
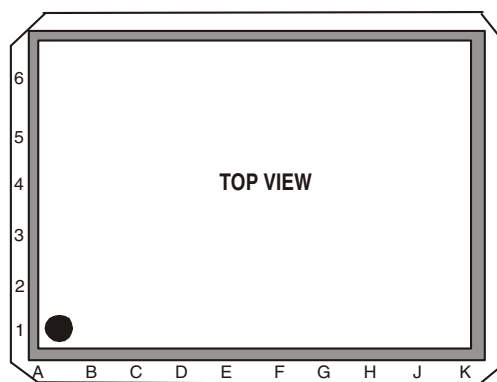
OCTOBER 2006

PIN CONFIGURATION

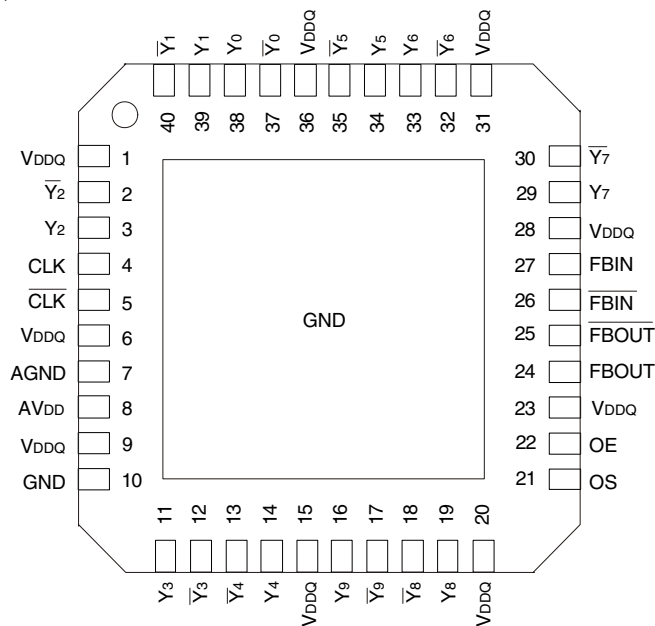
6	Y6	$\overline{Y6}$	$\overline{Y7}$	Y7	FBIN	$\overline{FBIN}$	$\overline{FBOUT}$	FBOUT	Y8	$\overline{Y8}$
5	Y5	GND	GND	OS	VDDQ	OE	VDDQ	GND	GND	$\overline{Y9}$
4	$\overline{Y5}$	GND	NB	VDDQ	NB	NB	VDDQ	NB	GND	Y9
3	$\overline{Y0}$	GND	NB	VDDQ	NB	NB	VDDQ	NB	GND	Y4
2	Y0	GND	GND	VDDQ	VDDQ	VDDQ	VDDQ	GND	GND	$\overline{Y4}$
1	Y1	$\overline{Y1}$	$\overline{Y2}$	Y2	CLK	$\overline{CLK}$	AGND	AVDD	Y3	$\overline{Y3}$
	A	B	C	D	E	F	G	H	J	K

VFBGA  
TOP VIEW

52 BALL VFBGA PACKAGE LAYOUT



PIN CONFIGURATION, CONT.



VQFPN  
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1,2)

Symbol	Rating	Max	Unit
VDDQ, AVDD	Supply Voltage Range	-0.5 to +2.5	V
VI(3)	Input Voltage Range	-0.5 to VDDQ + 0.5	V
VO(3)	Voltage range applied to any output in the high or low state	-0.5 to VDDQ + 0.5	V
I <sub>IK</sub> (VI < 0)	Input clamp current	±50	mA
I <sub>OK</sub> (VO < 0 or VO > VDDQ)	Output Clamp Current	±50	mA
I <sub>O</sub> (VO = 0 to VDDQ)	Continuous Output Current	±50	mA
VDDQ or GND	Continuous Current	±100	mA
TSTG	Storage Temperature Range	- 65 to +150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
3. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 2.5V max.

CAPACITANCE(1)

Parameter	Description	Min.	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance VI = VDDQ or GND	2	—	3	pF
C <sub>IΔ</sub>	Delta Input Capacitance CLK, CLK, FBIN, FBIN			0.25	pF
C <sub>L</sub>	Load Capacitance	—	10	—	pF

NOTE:

1. Unused inputs must be held high or low to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD(1)	Supply Voltage		VDDQ		V
VDDQ	I/O Supply Voltage	1.7	1.8	1.9	V
TA	Operating Free-Air Temperature	0	—	+70	°C

- NOTE:
1. The PLL is turned off and bypassed for test purposes when AVDD is grounded. During this test mode, VDDQ remains within the recommended operating conditions and no timing parameters are guaranteed.

### PIN DESCRIPTION (VFBGA)

Pin Name	Pin Number	Description
AGND	G1	Ground for 1.8V analog supply
AV <sub>DD</sub>	H1	1.8V analog supply
CLK, $\overline{\text{CLK}}$	E1, F1	Differential clock input with a 10K $\Omega$ to 100K $\Omega$ pulldown resistor
FBIN, $\overline{\text{FBIN}}$	E6, F6	Feedback differential clock input
$\overline{\text{FBOU}}$ , FBOU	G6, H6	Feedback differential clock output
GND	B2 - B5, C2, C5, H2, H5, J2 - J5	Ground
V <sub>DDQ</sub>	D2 - D4, E2, E5, F2, G2 - G5	1.8V supply
OE	F5	Output Enable
OS	D5	Output Select (tied to GND or V <sub>DDQ</sub> )
$\overline{\text{Y}}_{[0:9]}$	A3, A4, B1, B6, C1, C6, K1, K2, K5, K6	Buffered output of input clock, $\overline{\text{CLK}}$
Y <sub>[0:9]</sub>	A1, A2, A5, A6, D1, D6, J1, J6, K3, K4	Buffered output of input clock, CLK
NB		No Ball

### PIN DESCRIPTION (VFQFPN)

Pin Name	Pin Number	Description
AGND	7	Ground for 1.8V analog supply
AV <sub>DD</sub>	8	1.8V analog supply
CLK, $\overline{\text{CLK}}$	4, 5	Differential clock input with a 10K $\Omega$ to 100K $\Omega$ pulldown resistor
FBIN, $\overline{\text{FBIN}}$	26, 27	Feedback differential clock input
$\overline{\text{FBOU}}$ , FBOU	24, 25	Feedback differential clock output
GND	10	Ground
V <sub>DDQ</sub>	1, 6, 9, 15, 20, 23, 28, 31, 36	1.8V supply
OE	22	Output Enable
OS	21	Output Select (tied to GND or V <sub>DDQ</sub> )
Y <sub>[0:9]</sub>	3, 11, 14, 16, 19, 29, 33, 34, 38, 39	Buffered output of input clock, CLK
$\overline{\text{Y}}_{[0:9]}$	2, 12, 13, 17, 18, 30, 32, 35, 37, 40	Buffered output of input clock, $\overline{\text{CLK}}$
NB		No Ball

FUNCTION TABLE<sup>(1,2)</sup>

INPUTS					OUTPUTS				PLL
AV <sub>DD</sub>	OE	OS	CLK	$\overline{\text{CLK}}$	Y	$\overline{\text{Y}}$	F <sub>BOUT</sub>	$\overline{\text{F}}_{\text{BOUT}}$	
GND	H	X	L	H	L	H	L	H	OFF
GND	H	X	H	L	H	L	H	L	OFF
GND	L	H	L	H	L(z)	L(z)	L	H	OFF
GND	L	L	H	L	L(z) Y <sub>7</sub> Active	L(z) $\overline{\text{Y}}_7$ Active	H	L	OFF
1.8V (nom)	L	H	L	H	L(z)	L(z)	L	H	ON
1.8V (nom)	L	L	H	L	L(z) Y <sub>7</sub> Active	L(z) $\overline{\text{Y}}_7$ Active	H	L	ON
1.8V (nom)	H	X	L	H	L	H	L	H	ON
1.8V (nom)	H	X	H	L	H	L	H	L	ON
1.8V (nom)	X	X	L <sup>(3)</sup>	L <sup>(3)</sup>	L(z)	L(z)	L(z)	L(z)	OFF
X	X	X	H	H	Reserved				

NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care
- L(z) means the outputs are disabled to a LOW state, meeting the I<sub>ODL</sub> limit in DC Electrical Characteristics table.
- The device will enter a low power-down mode when CLK and  $\overline{\text{CLK}}$  are both at logic LOW.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>IK</sub>	Input Clamp Voltage (All Inputs)	V <sub>DDQ</sub> = 1.7V, I <sub>I</sub> = -18mA	—	—	-1.2	V
V <sub>IL</sub> ( <sup>2</sup> )	Input LOW Voltage (OE, OS, CLK, $\overline{\text{CLK}}$ )		—	—	0.35V <sub>DDQ</sub>	V
V <sub>IH</sub> ( <sup>2</sup> )	Input HIGH Voltage (OE, OS, CLK, $\overline{\text{CLK}}$ )		0.65V <sub>DDQ</sub>	—	—	
V <sub>IN</sub> ( <sup>1</sup> )	Input Signal Voltage		-0.3	—	V <sub>DDQ</sub> + 0.3	V
V <sub>ID</sub> (DC)( <sup>2</sup> )	DC Input Differential Voltage		0.3		V <sub>DDQ</sub> + 0.4	V
V <sub>OD</sub> ( <sup>3</sup> )	Output Differential Voltage	AV <sub>DD</sub> /V <sub>DDQ</sub> = 1.7V	0.6	—	—	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100μA, V <sub>DDQ</sub> = 1.7V to 1.9V	V <sub>DDQ</sub> - 0.2		—	V
		I <sub>OH</sub> = -9mA, V <sub>DDQ</sub> = 1.7V	1.1		—	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 100μA, V <sub>DDQ</sub> = 1.7V to 1.9V			0.1	V
		I <sub>OL</sub> = 9mA, V <sub>DDQ</sub> = 1.7V			0.6	
I <sub>ODL</sub>	Output Disabled LOW Current	OE = L, V <sub>ODL</sub> = 100mV, AV <sub>DD</sub> /V <sub>DDQ</sub> = 1.7V	100	—	—	μA
I <sub>IN</sub>	Input Current	CLK, $\overline{\text{CLK}}$			±250	μA
		OE, OS, FBIN, $\overline{\text{FBIN}}$			±10	
I <sub>DDL</sub>	Static Supply Current (I <sub>DDQ</sub> and I <sub>ADD</sub> )	AV <sub>DD</sub> /V <sub>DDQ</sub> = Max., CLK and $\overline{\text{CLK}}$ = GND			500	μA
I <sub>DD</sub>	Dynamic Power Supply Current (I <sub>DDQ</sub> and I <sub>ADD</sub> )( <sup>4,5</sup> )	AV <sub>DD</sub> /V <sub>DDQ</sub> = Max., CLK = 410MHz			300	mA

## NOTES:

- V<sub>IN</sub> specifies the allowable DC excursion of each different output.
- V<sub>ID</sub> is the magnitude of the difference between the input level on CLK and the input level on  $\overline{\text{CLK}}$ . The CLK and  $\overline{\text{CLK}}$  V<sub>IH</sub> and V<sub>IL</sub> limits are used to define the DC LOW and HIGH levels for the power down mode.
- V<sub>OD</sub> is the magnitude of the difference between the true output level and the complementary level.
- All Outputs are left open (unconnected to PCB).
- Total I<sub>DD</sub> = I<sub>DDQ</sub> + I<sub>ADD</sub> = F<sub>CK</sub> \* C<sub>PD</sub> \* V<sub>DDQ</sub>, for C<sub>PD</sub> = (I<sub>DDQ</sub> + I<sub>ADD</sub>) / (F<sub>CK</sub> \* V<sub>DDQ</sub>) where F<sub>CK</sub> is the input frequency, V<sub>DDQ</sub> is the power supply, and C<sub>PD</sub> is the Power Dissipation Capacitance.

## TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit
f <sub>CLK</sub>	Operating Clock Frequency( <sup>1,2,5</sup> )	125	410	MHz
	Application Clock Frequency( <sup>1,3,5</sup> )	160	410	MHz
t <sub>DC</sub>	Input Clock Duty Cycle	40	60	%
t <sub>L</sub>	Stabilization Time( <sup>4</sup> )	—	6	μs

## NOTES:

- The PLL will track a spread spectrum clock input.
- Operating clock frequency is the range over which the PLL will lock, but may not meet all timing specifications. To be used only for low speed system debug.
- Application clock frequency is the range over which timing specifications apply.
- Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the PLL circuit to obtain phase lock of its feedback signal to its reference signal when CLK and  $\overline{\text{CLK}}$  go to a logic LOW state, enters the power-down mode, and later return to active operation. CLK and  $\overline{\text{CLK}}$  may be left floating after they have been driven LOW for one complete clock cycle.
- Will lock to input frequency as low as 30MHz at room temperature and nominal or higher supply voltage (1.8V - 1.9V).

AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

Symbol	Description	f <sub>clk</sub> (MHz)	Min.	Typ. <sup>(2)</sup>	Max.	Unit
t <sub>EN</sub>	OE to any Y/Ȳ	160 to 410	—	—	8	ns
t <sub>DIS</sub>	OE to any Y/Ȳ	160 to 410	—	—	8	ns
SLR(I)	Output Enable ( $\overline{OE}$ )	160 to 410	0.5	—	—	V/ns
	Input Clock Slew Rate, measured single-ended	160 to 410	1	2.5	4	
SLR(O) <sup>(4)</sup>	Output Clock Slew Rate, measured single-ended	160 to 410	1.5	2.5	3	V/ns
V <sub>OX</sub> <sup>(6)</sup>	Output Differential-Pair Cross-Voltage	160 to 410	(V <sub>DDO</sub> /2) - 0.1	—	(V <sub>DDO</sub> /2) + 0.1	V
t <sub>JIT</sub> (CC+)	Cycle-to-Cycle Period Jitter	160 to 410	0	—	40	ps
t <sub>JIT</sub> (CC-)	Cycle-to-Cycle Period Jitter	160 to 410	0	—	-40	ps
t <sub>(∅)</sub> <sup>(5)</sup>	Static Phase Offset	160 to 410	-50	—	50	ps
t <sub>(∅)DYN</sub> <sup>(7)</sup>	Dynamic Phase Offset	160 to 270	-50	—	50	ps
		271 to 410	t <sub>(∅)DYN</sub> (MIN)	—	t <sub>(∅)DYN</sub> (MAX)	
tsk(O) <sup>(7)</sup>	Output Clock Skew	160 to 270	—	—	40	ps
		271 to 410	—	—	tsk(O)MAX	
t <sub>JIT</sub> (PER) <sup>(3,7)</sup>	Period Jitter	160 to 270	-40	—	40	ps
		271 to 410	t <sub>JIT</sub> (PER)MIN	—	t <sub>JIT</sub> (PER)MAX	
t <sub>JIT</sub> (HPER) <sup>(3)</sup>	Half-Period Jitter	160 to 270	-75	—	75	ps
		271 to 410	-50	—	50	
Σt(SU) <sup>(7)</sup>	t <sub>JIT</sub> (PER)   +   t <sub>(∅)DYN</sub>   + tsk(O)	271 to 410	—	—	80	ps
Σt(H) <sup>(7)</sup>	t <sub>(∅)DYN</sub>   + tsk(O)	271 to 410	—	—	60	ps
The PLL on the CSPUA877A will meet all the above test parameters while supporting SSC synthesizers with the following parameters:						
	SSC Modulation Frequency		30	—	33	KHz
	SSC Clock Input Frequency Deviation		0	—	0.5	%
CSPUA877A PLL designs should target the value below to minimize SSC-induced skew:						
	PLL Loop Bandwidth (-3dB from unity gain)		2	—	—	MHz

## NOTES:

- There are two different terminations that are used with the above AC tests. The output load shown in figure 1 is used to measure the input and output differential pair cross-voltage only. The output load shown in figure 2 is used to measure all other tests, including input and output slew rates. For consistency, use 50Ω equal length cables with SMA connectors on the test board.
- Refers to transition of non-inverting output.
- Period jitter and half-period jitter specifications are separate specifications that must be met independently of each other.
- To eliminate the impact of input slew rates on static phase offset, the input slew rates of reference clock input (CLK,  $\overline{CLK}$ ) and feedback clock input (FBIN,  $\overline{FBIN}$ ) are recommended to be nearly equal. The 2.5V/ns slew rates are shown as a recommended target. Compliance with these nominal values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
- Static phase offset does not include jitter.
- V<sub>OX</sub> is specified at the DDR DRAM clock input or test load.
- In the frequency range of 271 - 410MHz, the min and max values for t<sub>JIT</sub>(PER) and t<sub>(∅)DYN</sub>, and the max value for tsk(O), must not exceed the corresponding min and max values of the 160 - 270MHz range. Also, the sum of the specified values for | t<sub>JIT</sub>(PER) |, | t<sub>(∅)DYN</sub> |, and tsk(O) must meet the requirement for Σt(SU), and the sum of the specified values for | t<sub>(∅)DYN</sub> | and tsk(O) must meet the requirement for Σt(H).

TEST CIRCUIT AND SWITCHING WAVEFORMS

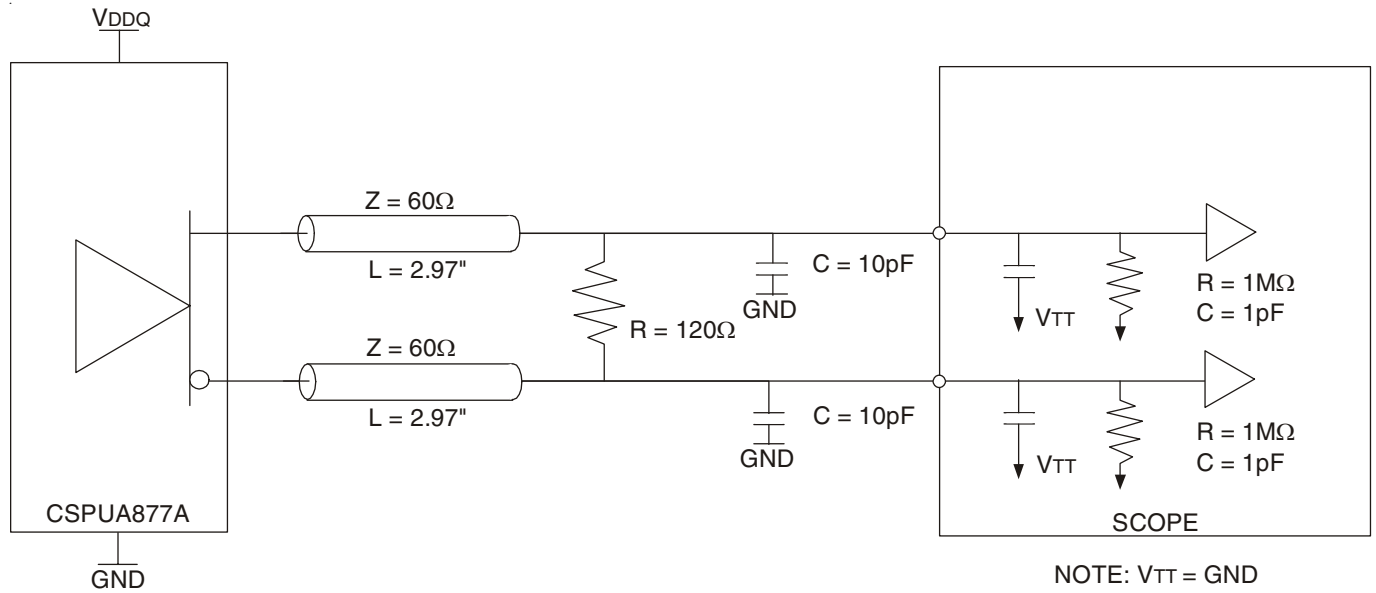


Figure 1: Output Load Test Circuit 1

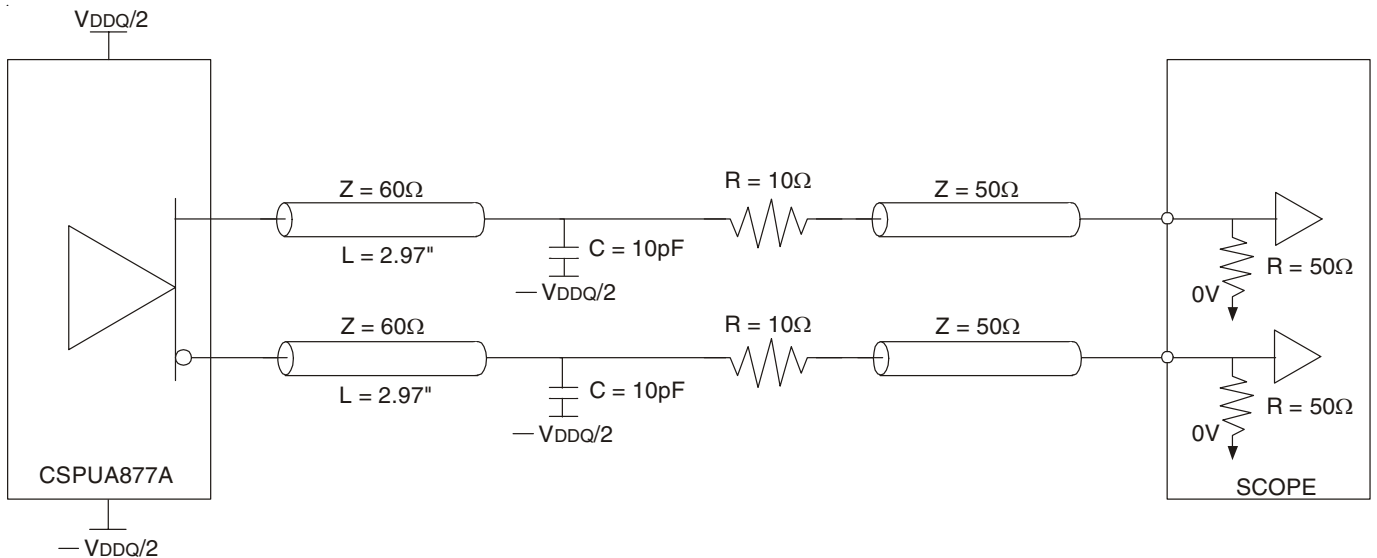
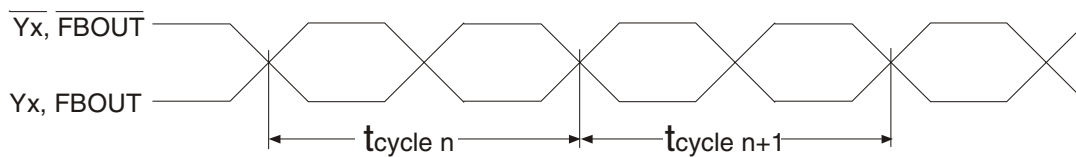


Figure 2: Output Load Test Circuit 2

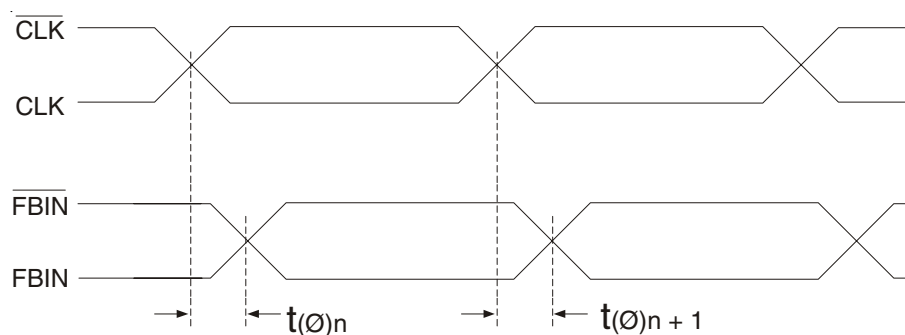


### TEST CIRCUIT AND SWITCHING WAVEFORMS



$$t_{\text{jit(cc)}} = t_{\text{cycle } n} - t_{\text{cycle } n+1}$$

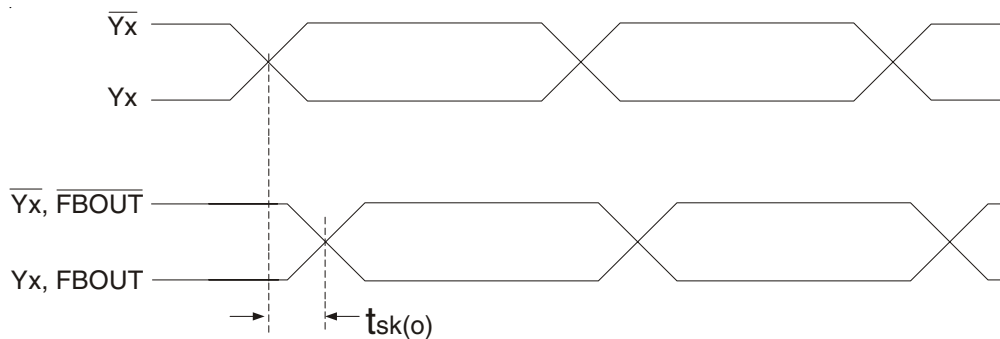
Cycle-to-Cycle jitter



$$t(\emptyset) = \frac{\sum_{n=1}^{n=N} t(\emptyset)_n}{N}$$

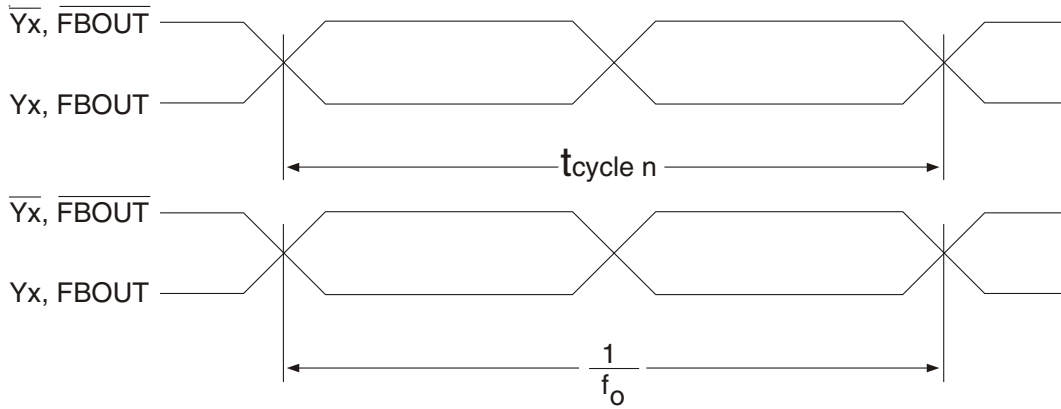
(N is a large number of samples)

Static Phase Offset



Output Skew

### TEST CIRCUIT AND SWITCHING WAVEFORMS

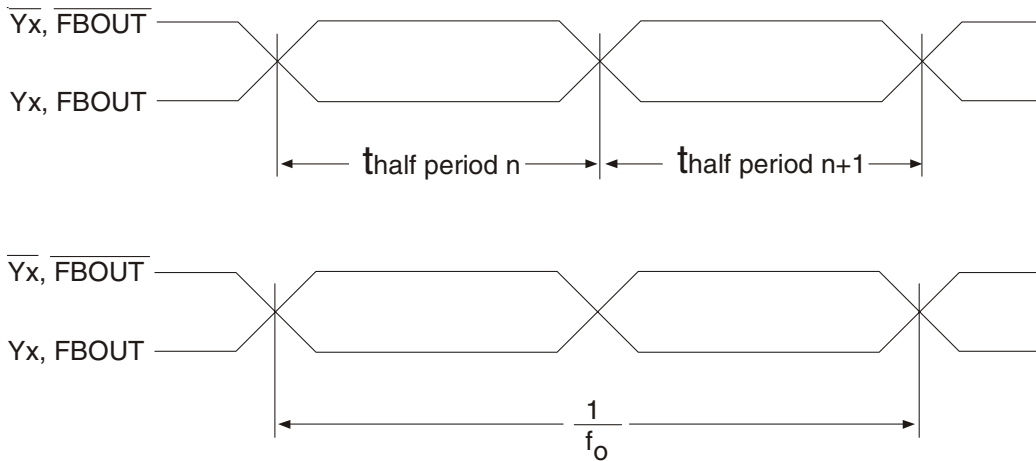


$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{f_0}$$

NOTE:

$f_0$  = Average input frequency measured at CLK /  $\overline{CLK}$

Period jitter



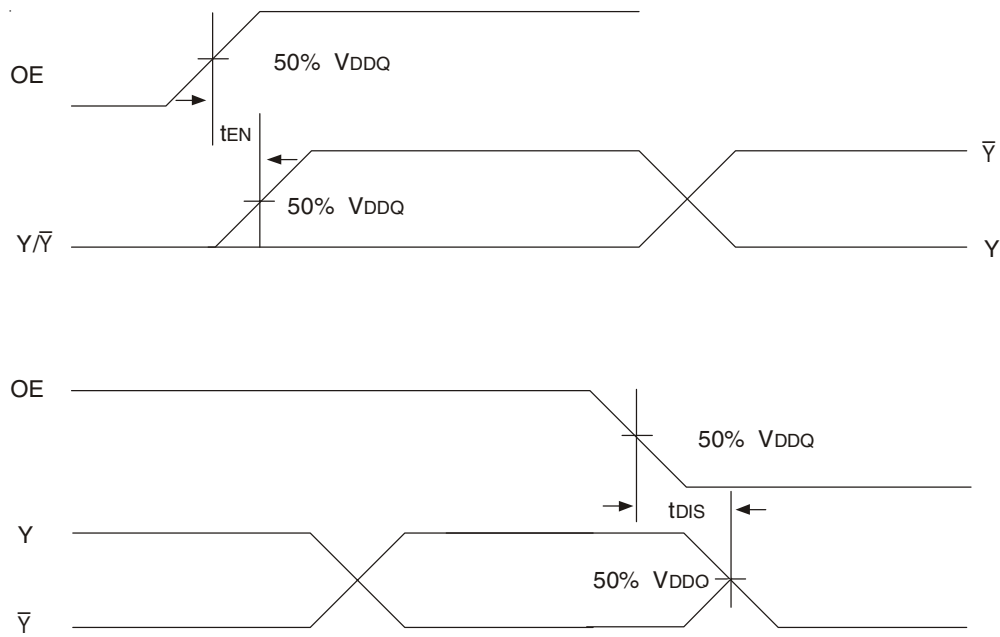
$$t_{jit(hper)} = t_{half\ period\ n} - \frac{1}{2 \cdot f_0}$$

NOTE:

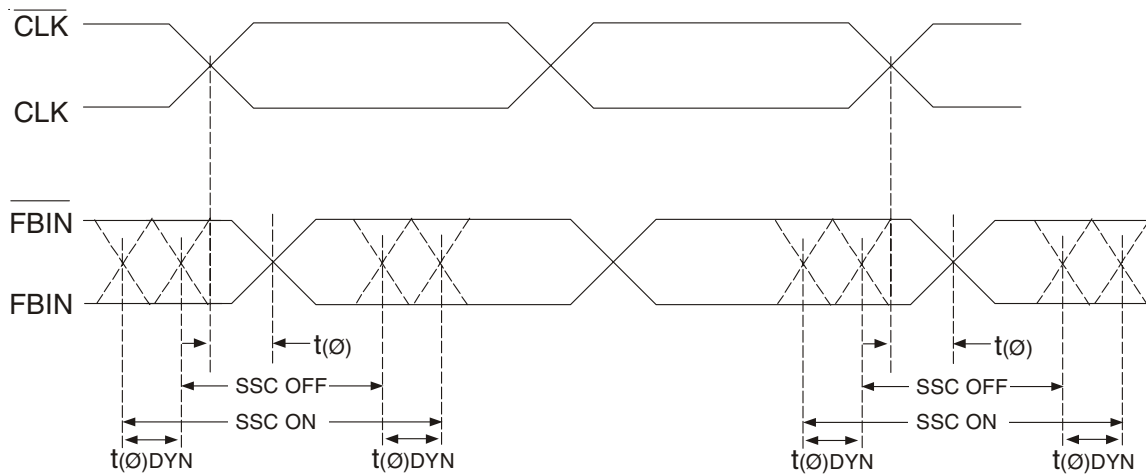
$f_0$  = Average input frequency measured at CLK /  $\overline{CLK}$

Half-Period jitter

TEST CIRCUIT AND SWITCHING WAVEFORMS

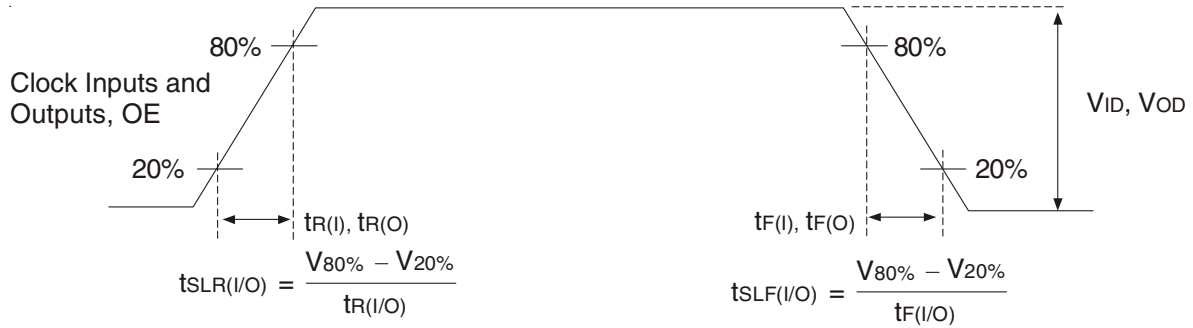


Time Delay Between Output Enable (OE) and Clock Output (Y, Y-bar)

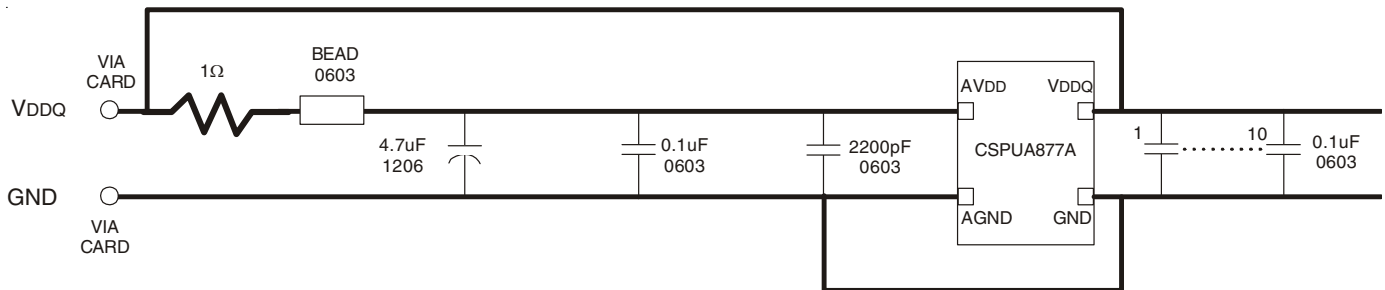


Dynamic Phase Offset

## TEST CIRCUIT AND SWITCHING WAVEFORMS



Input and Output Slew Rates



**NOTES:**

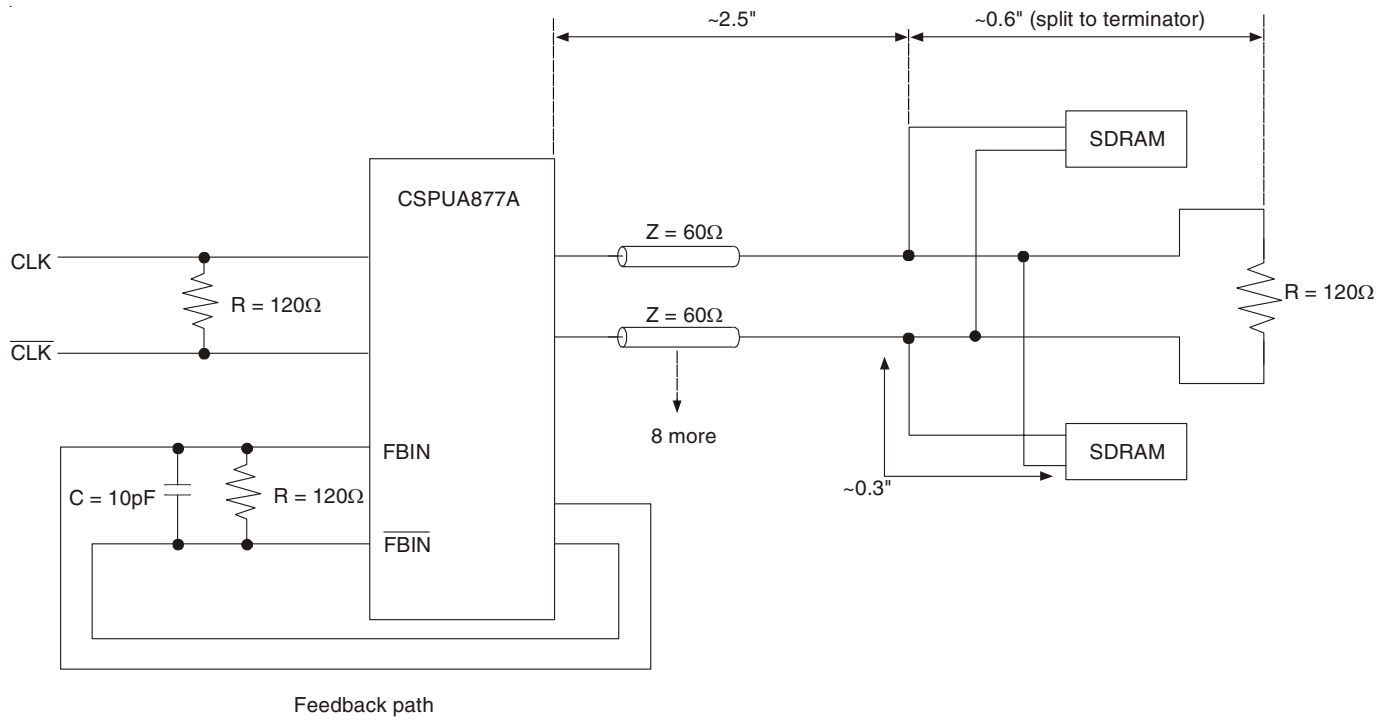
- Place all decoupling capacitors as close to the CSPA877A pins as possible.
- Use wide traces for AVDD and AGND.
- Recommended bead: Fair-rite P/N 2506036017Y0 or equivalent (0.8Ω DC max., 600Ω at 100MHz).

Recommended Filtering for the Analog and Digital Power Supplies (AVDD and VDDQ)

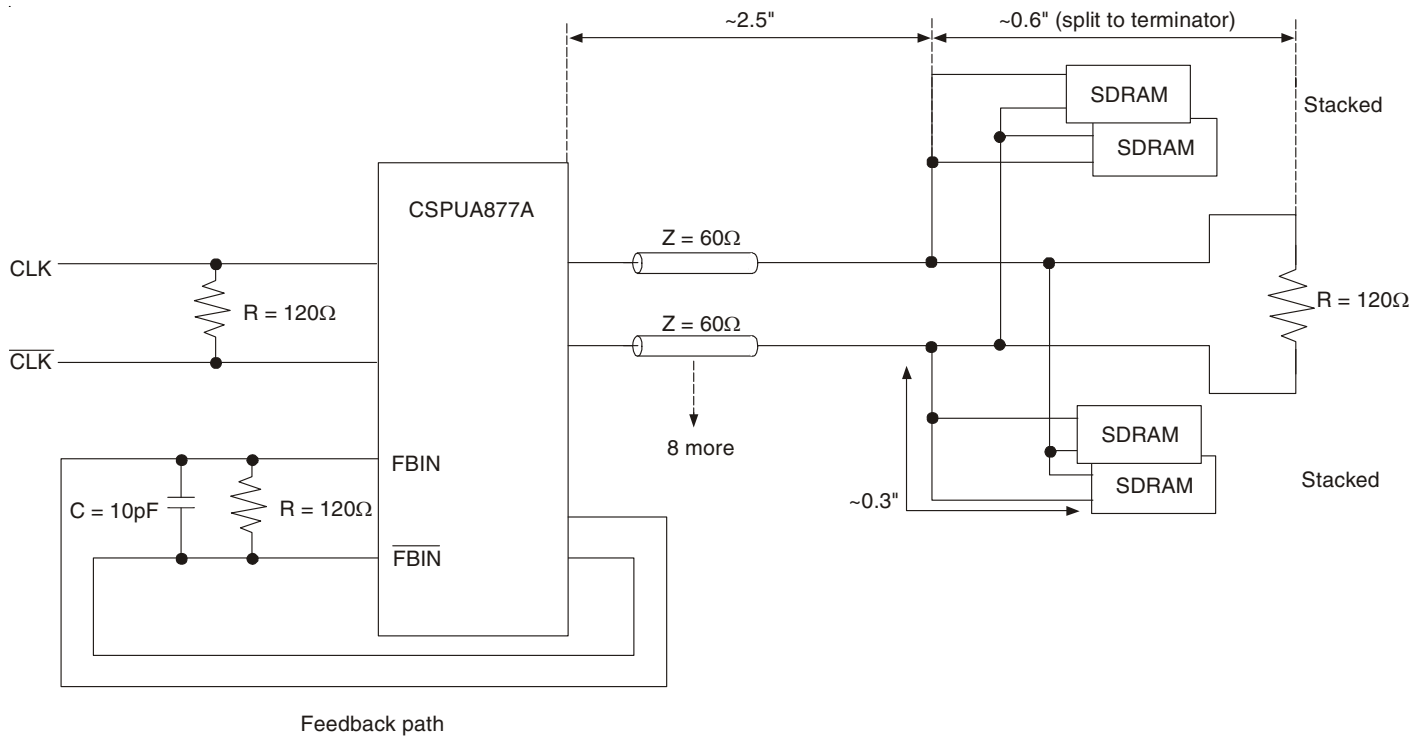
## APPLICATION INFORMATION

Clock Structure	# of SDRAM Loads per Clock	Clock Loading on the PLL outputs (pF)	
		Min.	Max.
#1	2	3	5
#2	4	6	10

APPLICATION INFORMATION



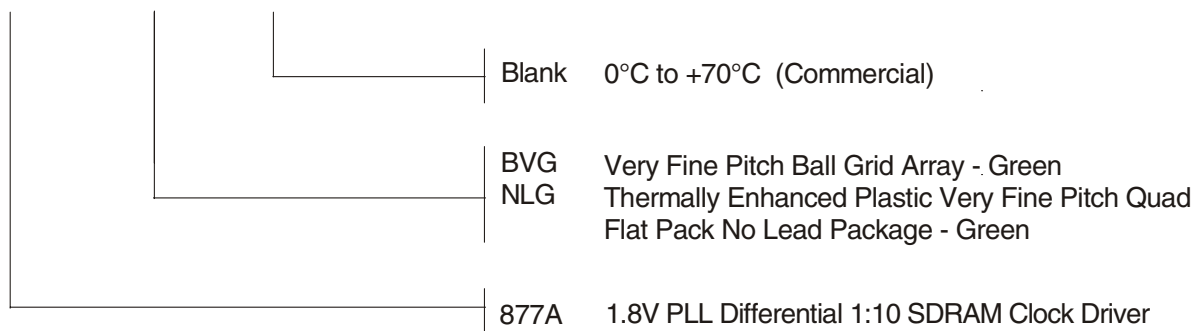
Clock Structure 1



Clock Structure 2

## ORDERING INFORMATION

IDTCSPUA XXXXX XX X  
Device Type Package Process



**CORPORATE HEADQUARTERS**  
6024 Silver Creek Valley Road  
San Jose, CA 95138

**for SALES:**  
800-345-7015 or 408-284-8200  
fax: 408-284-2775  
www.idt.com

**for Tech Support:**  
logichelp@idt.com